

1. Structural Programming in VHDL

1.1 Structural Style

Structural Style Programming is an approach in VHDL that allows designers to create digital circuits by using basic components connected to each other to form a more complex system. In this approach, a circuit is represented as a collection of entities linked in a specific way to achieve the desired function.

1.2 Port Mapping

Port mapping is the process of associating (mapping) the ports of a component (entity) in VHDL with the signals present in the architecture. This allows us to connect a defined entity to the actual circuit in the design.

Some important points:

- **Entity Definition:** An entity must be defined before port mapping.
- **Port-Map List:** A list that maps ports to signals.
- **Port Mapping Order:** The order must match the entity's port definition.
- **Signal Declaration:** Signals must be declared beforehand.

Port Mapping Example

```
-- Entity definition
entity AND2 is
  port (
    A, B: in std_logic;
    Y: out std_logic
  );
end entity;

-- Port mapping in architecture (this is actually the entity's behavior)
```

```
architecture RTL of AND2 is
begin
    Y <= A and B;
end architecture;

-- Using the entity with port mapping in a higher-level design
D1: AND2 port map (
    A => input_signal_A,
    B => input_signal_B,
    Y => output_signal
);
```

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