1. Understanding Testbench in VHDL

A VHDL testbench is a non-synthesizable VHDL entity used to **simulate and verify the functionality** of another VHDL entity, often referred to as the Unit Under Test (UUT). Think of it as a **virtual lab environment** where you can apply a sequence of inputs (stimulus) to your design and observe its behavior and outputs over time. Since the testbench itself is not meant to be turned into a physical chip, it can use more abstract and powerful VHDL constructs that are not available for synthesizable hardware descriptions.

A testbench has many uses, including:

- Simplifying and speeding up the entity testing process because inputs do not need to be manually entered one by one through a simulation tool.
- Allowing the entity's output to be compared against predetermined values to verify its correctness.
- Enabling the test results to be saved into files, such as a .csv file, so they can be used by other software like Python, Excel, or MATLAB for further analysis.

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