

4. Array and Type

4.1 Array and Type in VHDL

4.1.1 Array

An array is a collection of elements of the same data type. It can be one-dimensional or multi-dimensional.

4.1.2 Type

A type is a new data definition. It can be a built-in type (`std_logic`, `integer`) or a user-derived type.

4.2 Type and Array Example

```
type RegisterArray is array (0 to 7) of std_logic_vector(7 downto 0);  
signal registers: RegisterArray := (others => (others => '0'));
```

Revision #1

Created 2025-09-24 13:02:27 UTC by AX

Updated 2025-09-24 13:03:37 UTC by AX