Final Project Guide

Congratulations! ?

In this final module, you are given the opportunity to create a project with your group members according to the following provisions:

Final Project Timeline

- **Github Link Deadline: Sunday, November 23, 2025 23.59 WIB**
- **Project Title:** Discuss with the supervising assistant (Must be decided by **Sunday, November 30, 2023**)
- **Project Submission Deadline: Sunday, December 7, 2025, 23:59 WIB**
- **Presentation Week: December 8-12, 2025** (discuss with the supervising assistant)

Final Project Criteria

- The final project must cover atleast 6 of the practicum modules. The program and testbench **MUST** use the VHDL language, including code explanations using comments.
- Create a **public GitHub repository** for project submission. Each individual must **commit regularly** so their individual contributions are visible in the final project (there will also be a contribution assessment form).
- You **must invite the supervising assistant** as a collaborator to the repo and to the LINE group.
- **Force pushing** to the repo is prohibited as it can delete commit history.
- You must create a **README.md** in the final project repository containing an explanation of your project. The sections can be the same as those in the report file, with the addition of code snippet explanations.
  - Tutorial: Markdown Crash Course.
  - Template: GitHub - matiassingers/awesome-readme
- **Program complexity** will affect the final project grade. If the project you create is limited to fulfilling module requirements and is less suitable for FPGA implementation, the grade will be lower than for one that is more suitable.
- **Example of a less suitable** (though not prohibited) project: Creating a Vending Machine can be implemented on an FPGA, or a DSD project you've done before can also be implemented with FPGA (VHDL). However, no one would implement something that simple on an FPGA because it's more practical to use an Arduino or another microcontroller.

- **Example of a more suitable** project: Creating a hardware accelerator for a specific, frequently used algorithm.
- Create a final project report based on the provided template.
- Create a presentation PowerPoint.

Final Project Grading Weight

- Report (PDF & MD): 15%
- Presentation (PPT, Delivery, & Q&A): 20%
- Complexity (including Understanding): 25%
- Idea Creativity: 10%
- Success/Functionality: 30%

Files and Submission Location

- **EMAS3**
  - GitHub Link (submitted on EMAS)
- **GitHub Repository**
  - PDF Report file
  - PPT Presentation file
  - Source code + Testbench
  - Quartus Synthesis
  - Modelsim waveform simulation
  - README.md

Example Final Project Ideas*

- **VHDL Image Processing:** Modify an image (e.g., Rotation, Brightness, Flip).
  - Source: https://github.com/juanjonathan67/Simple-Image-Augmenter
- **VHDL Image Upscaler:** Upscale an image.
  - Source: https://github.com/Jordinia/Bicubic-Interpolation
- **VHDL Enigma Encryption:** Encrypt an input message.
  - Source: https://github.com/ArmondHarer/Proyek-Akhir-PSD-B2

*Only use these three examples as a reference or for idea inspiration. **Plagiarism is prohibited**.

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