Quartus Prime Synthesis Tutorial

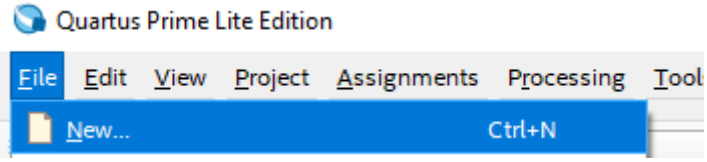
1.3 Quartus Prime Tutorial

For this tutorial, we will use this code for reference :

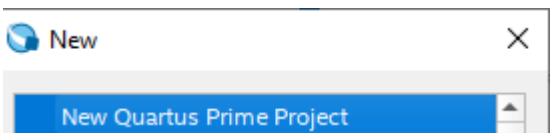
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY AND_GATE IS
    PORT (
        A : IN  STD_LOGIC;
        B : IN  STD_LOGIC;
        Y : OUT STD_LOGIC
    );
END AND_GATE;

ARCHITECTURE Behavioral OF AND_GATE IS
BEGIN
    Y <= A AND B;
END Behavioral;
```

1.3.1 Creating a New Quartus Prime Project

Create a new project by clicking new on file tab

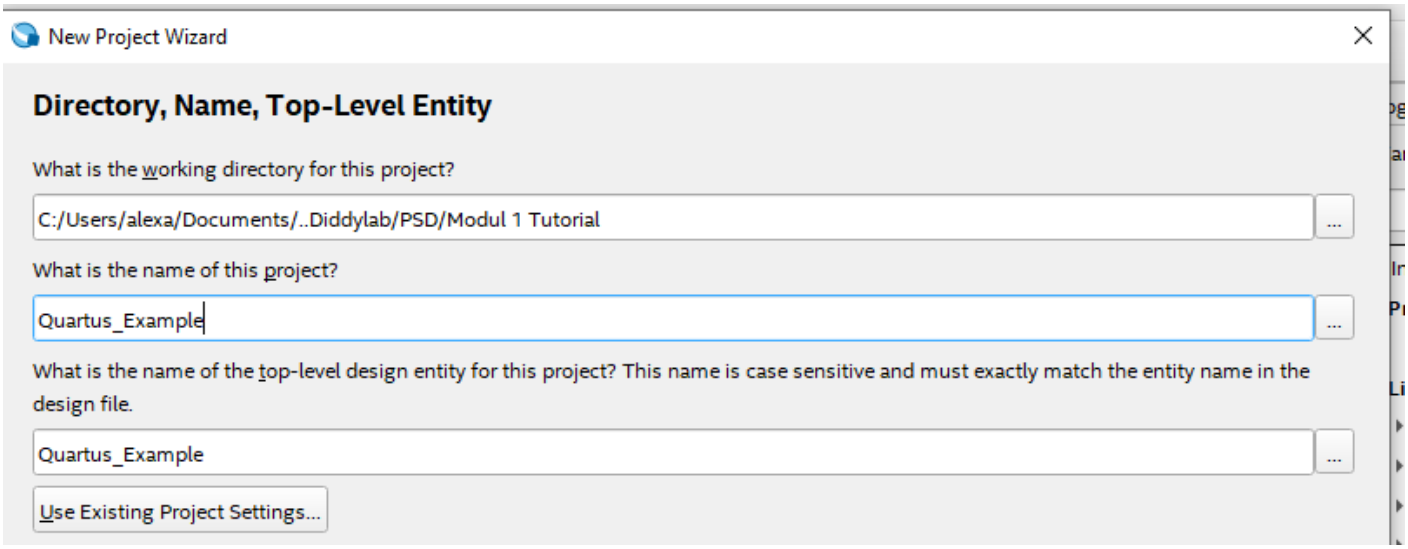


Select New Quartus Prime Project

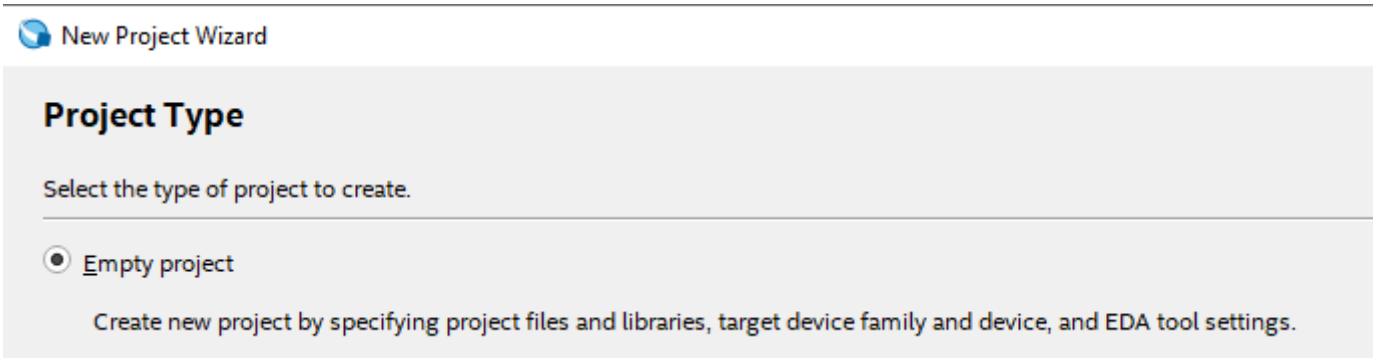


Select the directory where you want the project to be saved and also give the project a name and name your Top-Level Entity

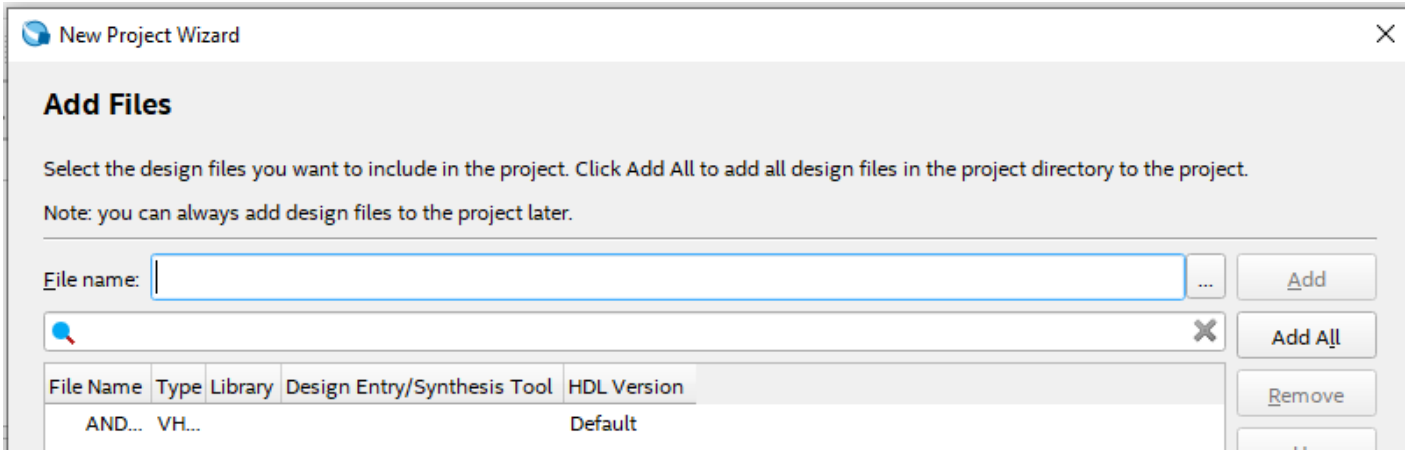
NOTE : Remember to name your Top-Level Entity into the same name as your Top-Level entity on your .vhdl



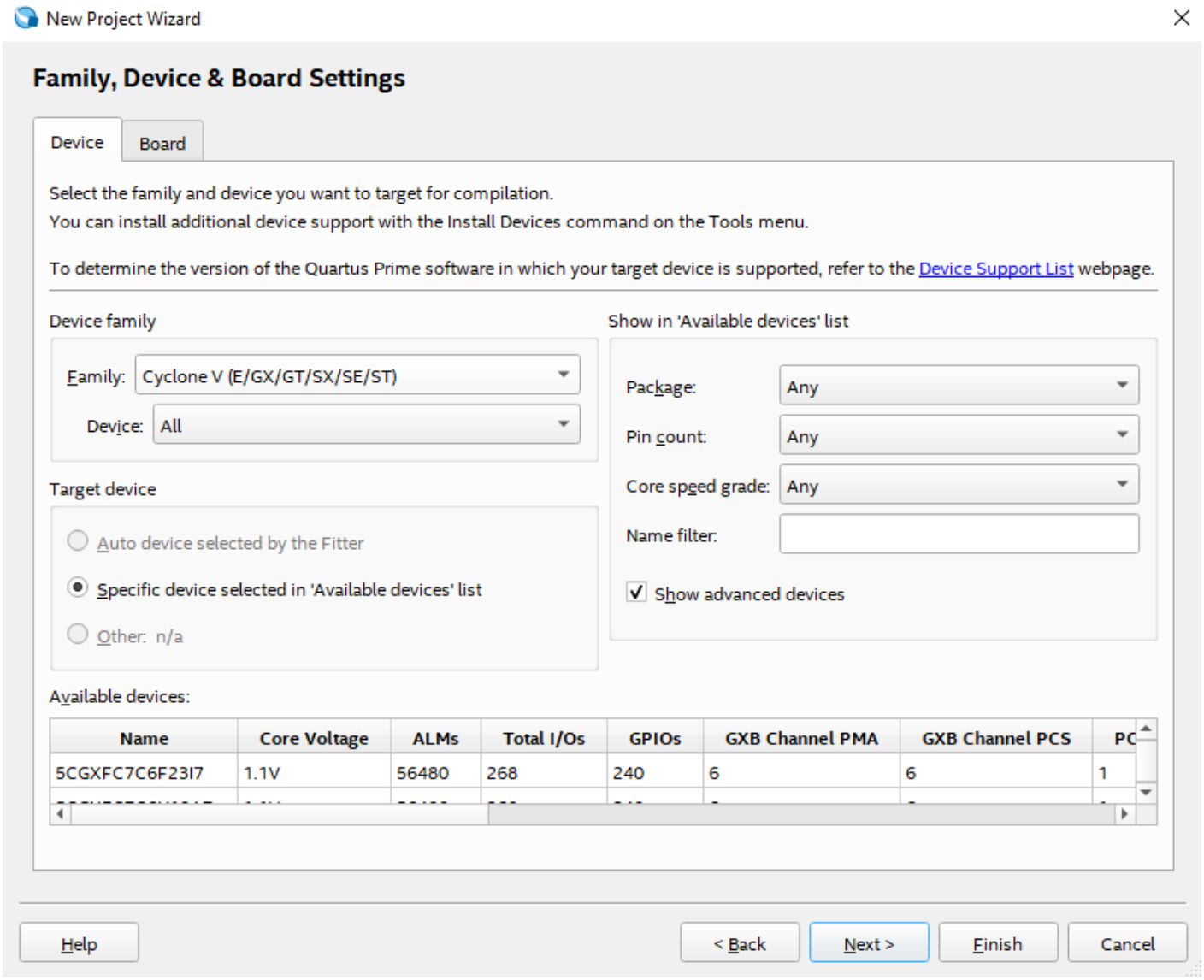
Choose empty project



Add your .vhdl/.vhd file into the project

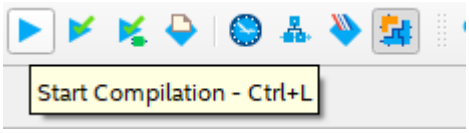


Just select the default setting and proceed to finish

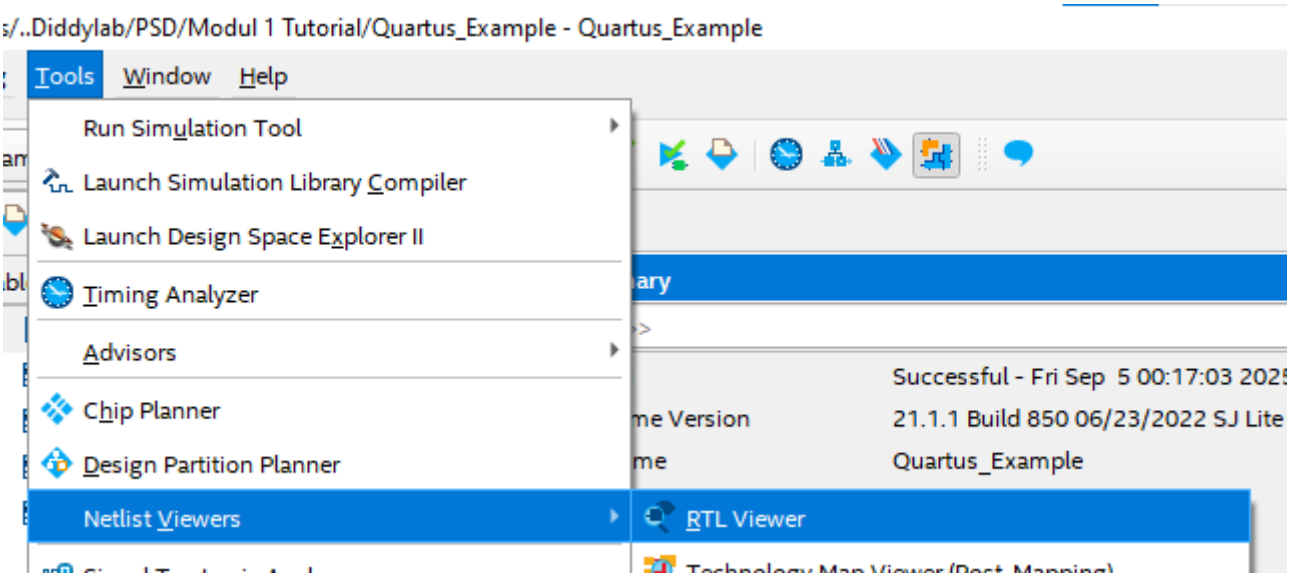


1.3.2 Synthesis Tutorial

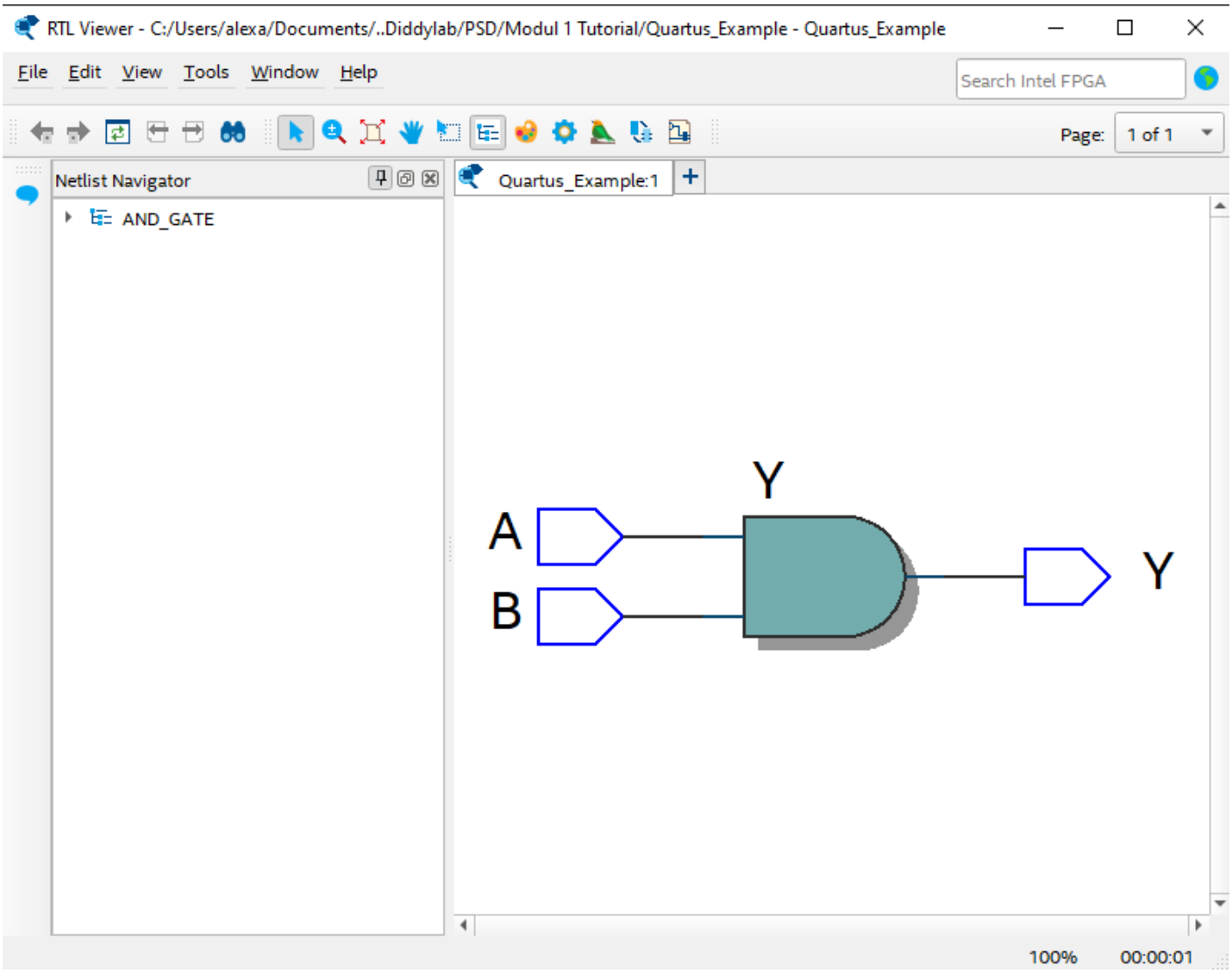
Run the "Start Compilation" button on top bar



Wait until the startup is finish and then go into Tools -> Netlist Viewers -> RTL Viewer



You may see your VHDL schematic



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