

# Vivado Simulation and Synthesis Tutorial

## 1.3 Vivado Tutorial

For this tutorial, we will use this code for reference :

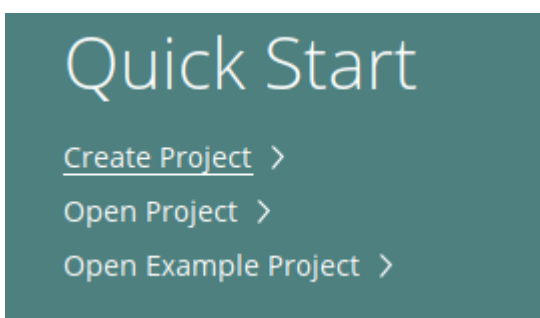
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY AND_GATE IS
    PORT (
        A : IN  STD_LOGIC;
        B : IN  STD_LOGIC;
        Y : OUT STD_LOGIC
    );
END AND_GATE;

ARCHITECTURE Behavioral OF AND_GATE IS
BEGIN
    Y <= A AND B;
END Behavioral;
```

### 1.3.1 Creating a new Vivado file

Create a new project



Enter your project name and where you want it to be saved

New Project

### Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

Create project subdirectory

Project will be created at: C:/Users/alexa/Documents/..Diddylab/PSD/Modul 1 Tutorial/Vivado\_Tutorial

## Choose RTL Project

New Project

### Project Type

Specify the type of project to create.

**RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

Do not specify sources at this time

Project is an extensible Vitis platform

**Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.

Do not specify sources at this time

**I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

**Imported Project**  
Create a Vivado project from a Synplify Project File.

**Example Project**  
Create a new Vivado project from a predefined template.

## Change the target language into VHDL and add your VHDL code into the project

Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Target language:

Simulator language:

## New Project

### Add Sources

Specify HDL, netlist, Block Design, a  
You can also add and create source



Add

### Add Source Files

Look in: Modul 1 Tutorial

Vivado\_Tutorial  
AND\_GATE.vhdl

#### Recent Directories

C:/Users/alexa/Documents/..Diddylab/PSD/Modul 1 Tutorial

#### File Preview

```
LIBRARY IEEE;  
USE IEEE.STD_LOGIC_1164.ALL;  
  
ENTITY AND_GATE IS  
  PORT (  
    A : IN  STD_LOGIC;  
    B : IN  STD_LOGIC;  
    Y : OUT STD_LOGIC  
  );  
END AND_GATE;  
  
ARCHITECTURE Behavioral OF AND_GATE IS  
BEGIN  
  Y <= A AND B;  
END Behavioral;
```

File name: AND\_GATE.vhdl

Files of type: Design Source Files (.vhd, .vhdl, .vhf, .vhdp, .vho, .v, .vf, .verilog, .vr, .vg, .vb, .tf, .vlog, .vp, .vm, .veo, .sv, .vh, .h, .svh, .vhp, .svhp, .edn, .edf, .edif, .ngc, .sv, .svp, .bmm, .mif, .mem, .elf, .dcp, .bd, .wcfg, .xco, .xci, .xcix)

OK

Cancel

## New Project

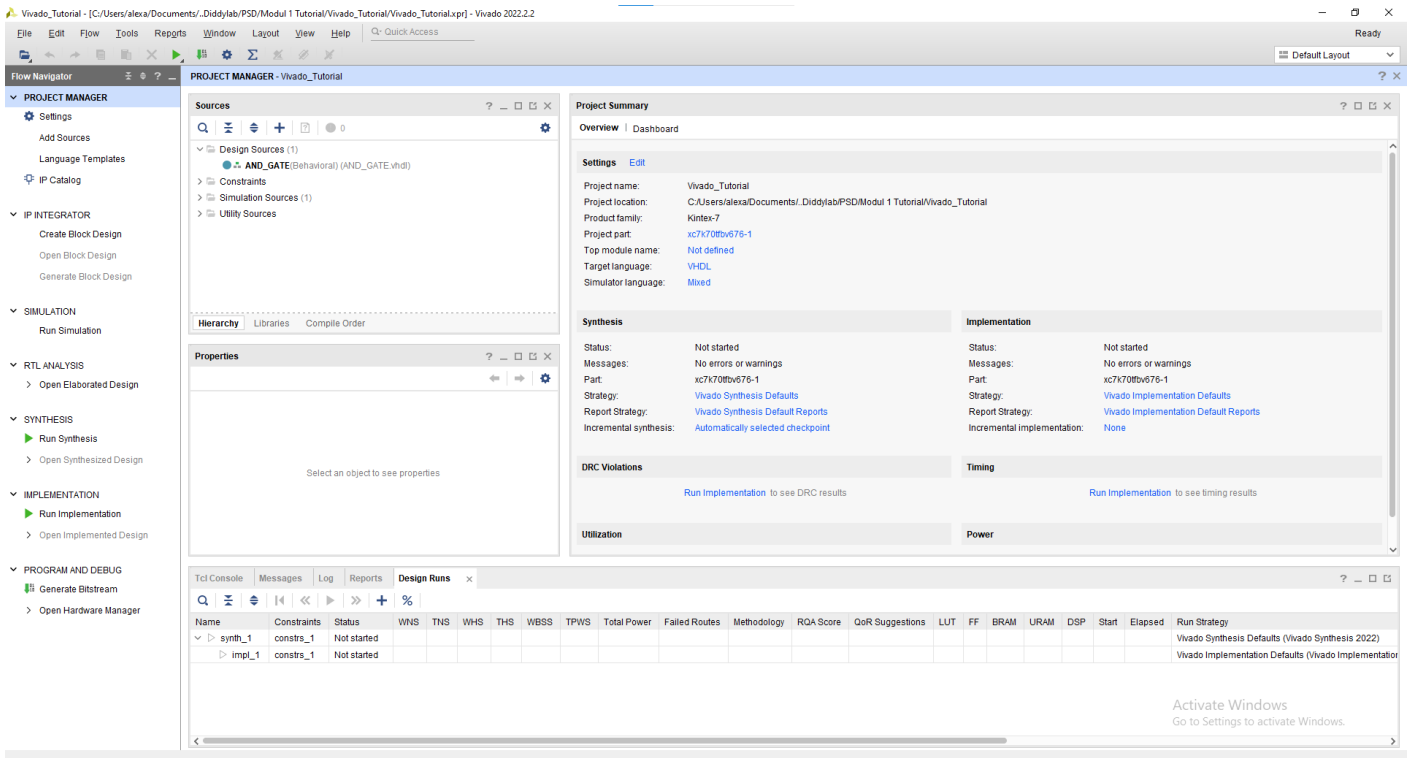
### Add Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project.  
You can also add and create sources later.



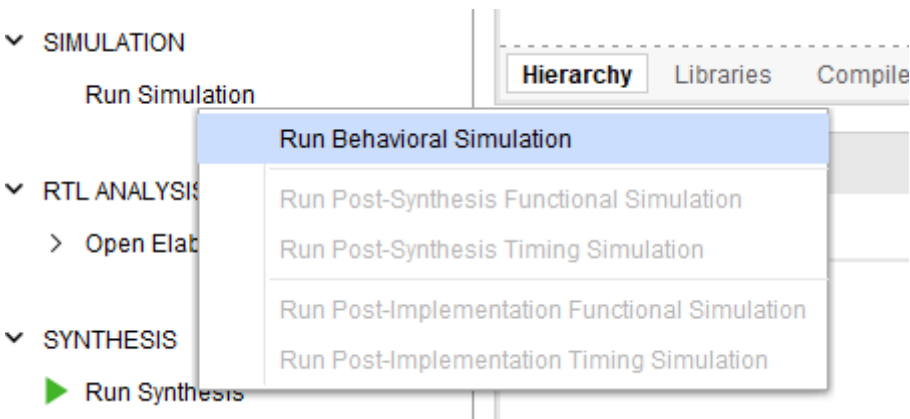
	Index	Name	Library	HDL Source For	Location
●	1	AND_GATE.vhdl	xil_defaultlib	Synthesis & Simulation	C:/Users/alexa/Documents/..Diddylab/PSD/Modul 1 Tutorial

You may skip the add constraints page and also the default part proceed into the project creation. Finally you've created a new project and this will be your screen now.



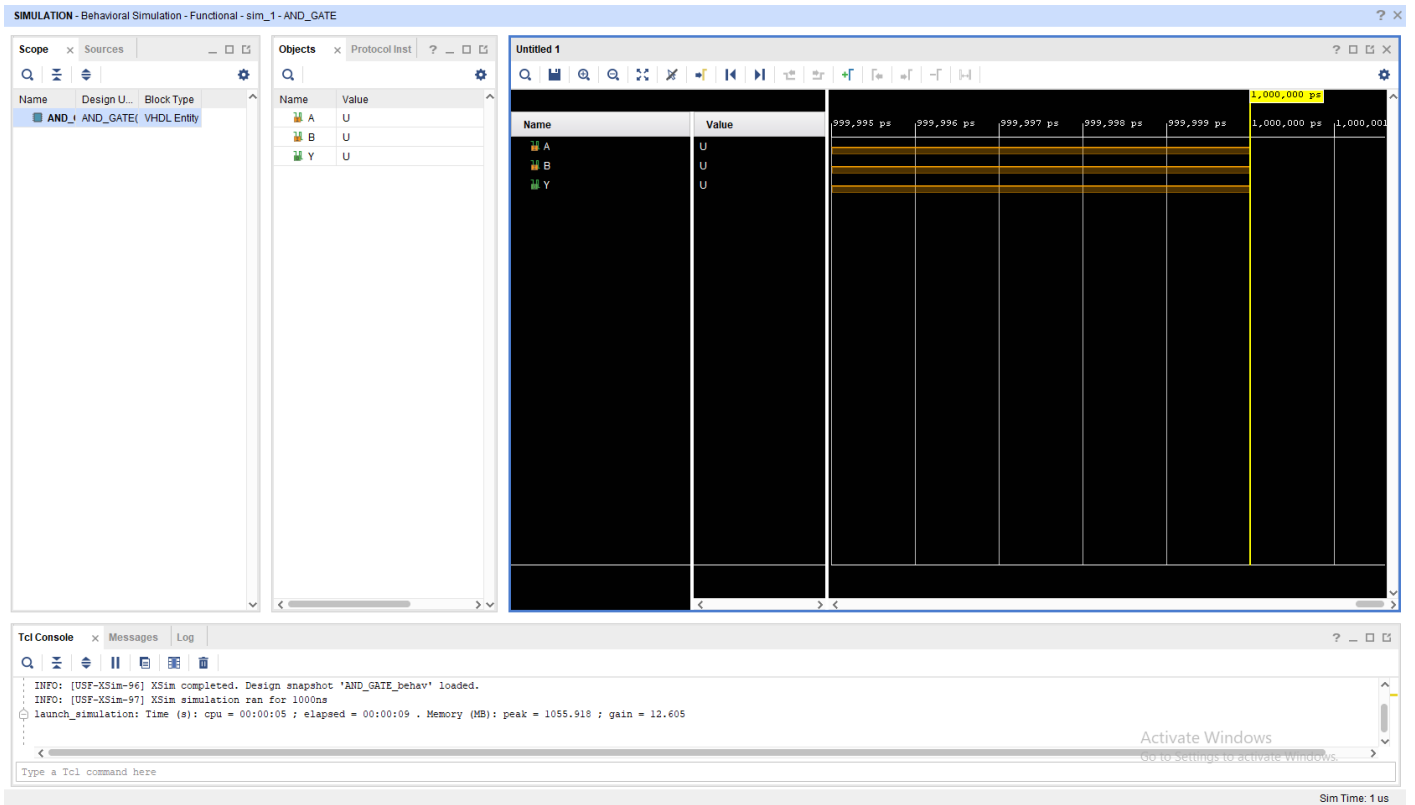
### 1.3.2 Simulation Tutorial

Click "Run Simulation" on the left part of the screen. And choose "Run Behavioral Simulation"

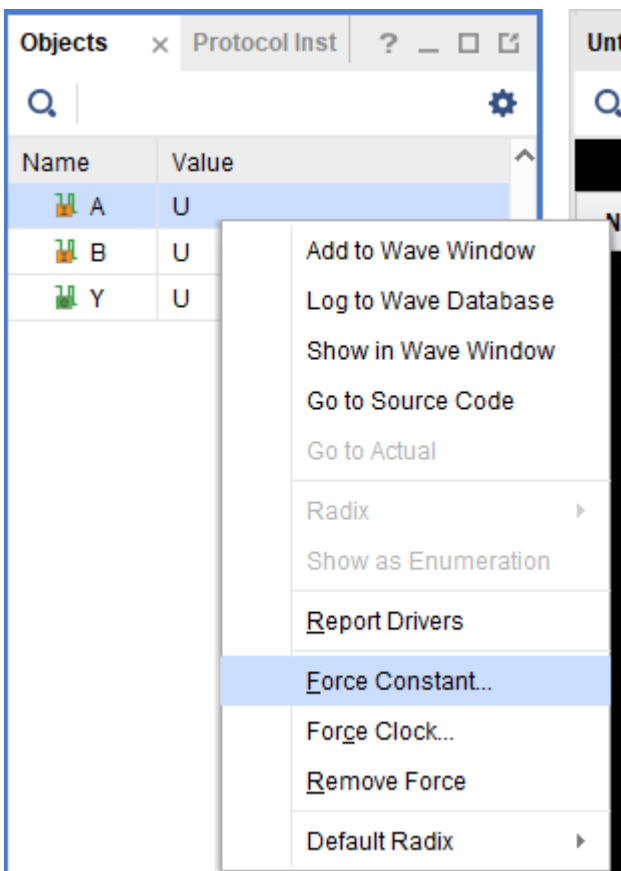


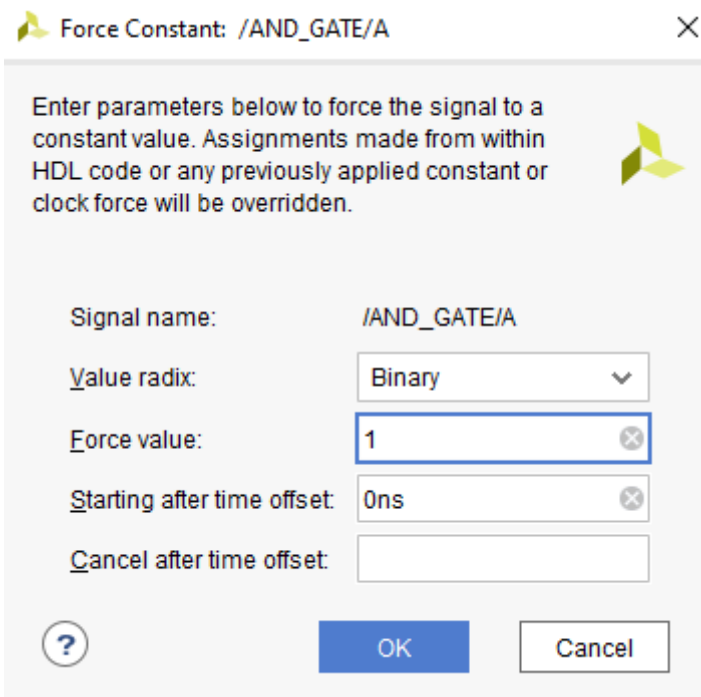
If there's any error warning, you may read and fix the error before proceeding into the simulation.

This will be your screen after you run the simulation.



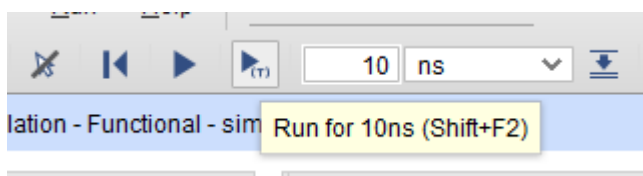
To add a signal, you may change the value in the objects part, choose "Force Constant" and change according to what you want to do. Remember to change the **INPUT** not the **OUTPUT**



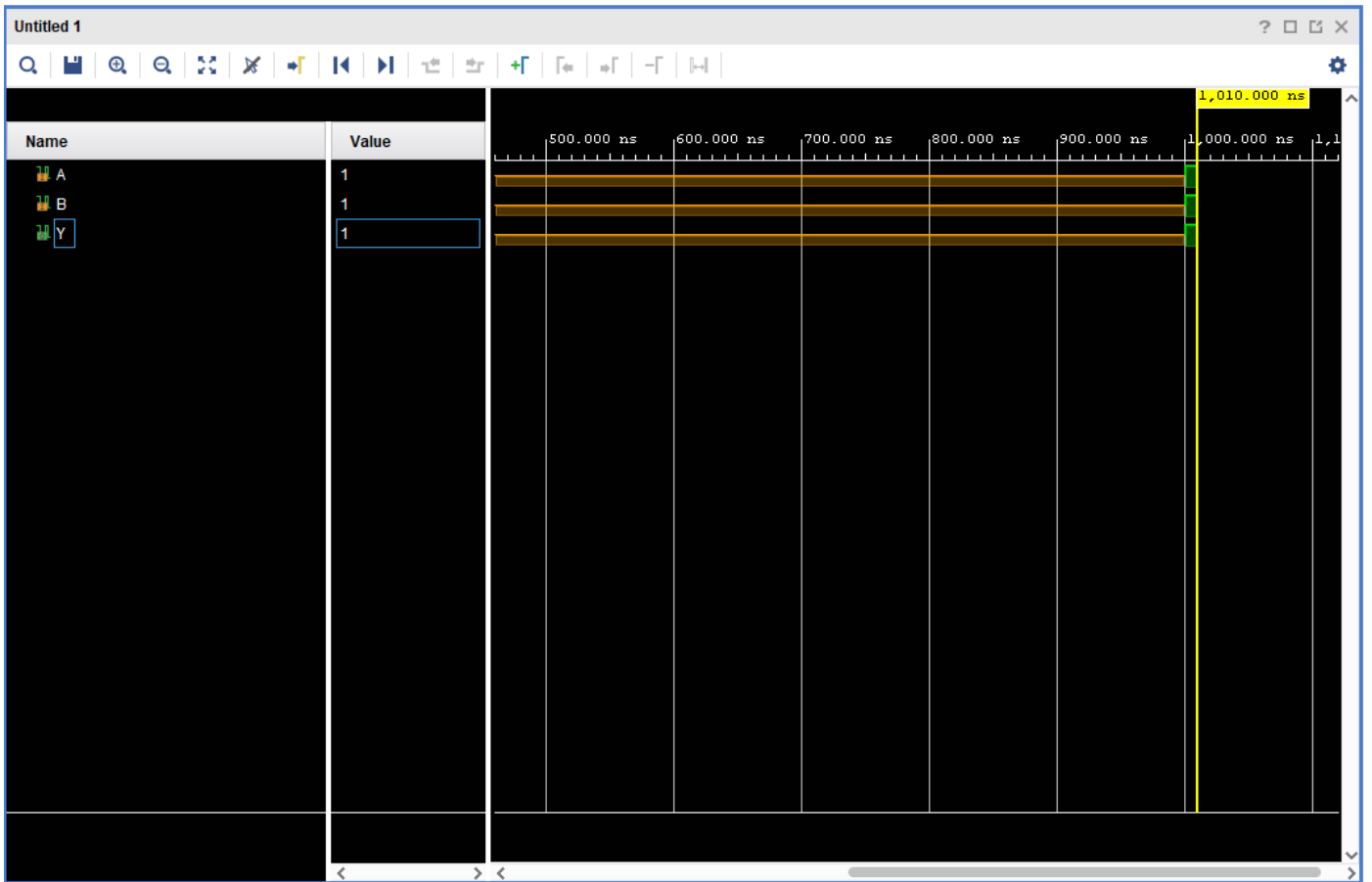


Name	Value
A	1
B	1
Y	U

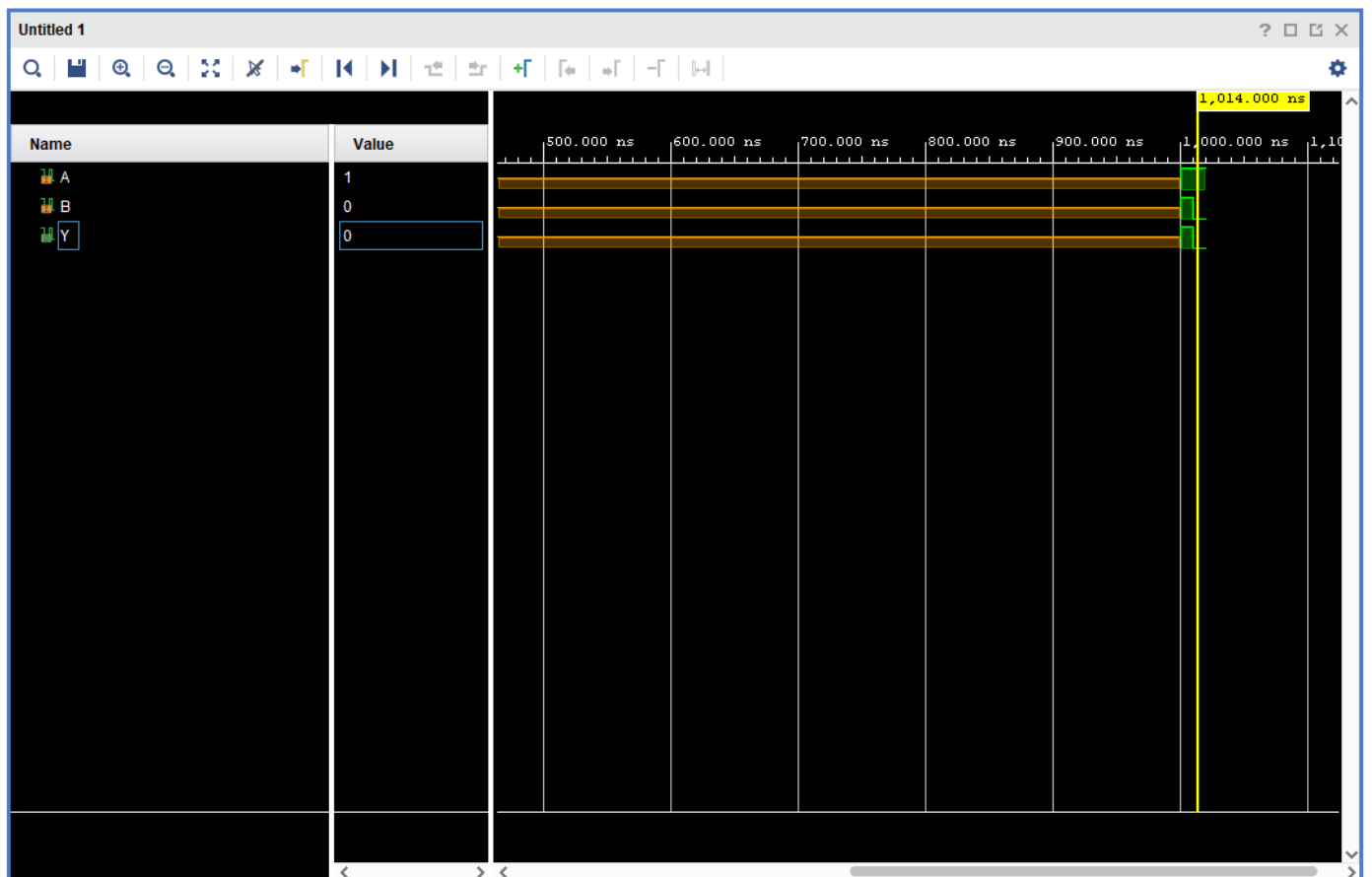
After changing the Value you may click the "Run for 10ns" on the top bar



You may see that there's a new signal after you press the button

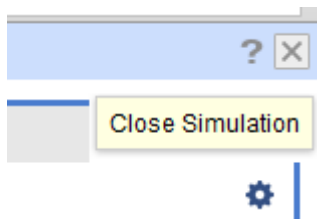


You may also move the yellow line with your cursor to switch to a different period of time on the waveform



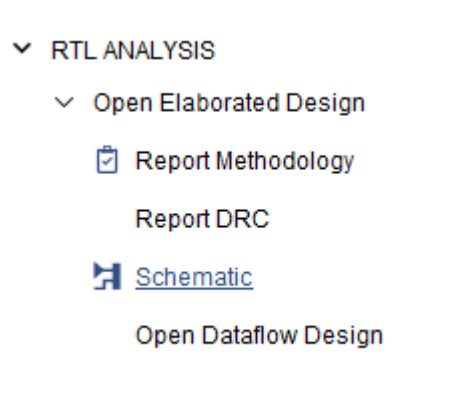
NOTE : All of this is just a manual simulation tutorial. There are a way to do this automatically (Hint: Module 4).

To close simulation, you may click the top right button



### 1.3.3 Synthesis Tutorial

Go to the "RTL Analysis" and run "Schematic" and if there's a notification just select "ok"



Wait until the elaborated design is finished and then you may see your VHDL code schematic.

