

# Testbench in Combinational Circuit

To use a testbench in a combinational circuit, you need to follow these steps:

## 1. We must have a VHDL code that to be tested.

```
library ieee;
use ieee.std_logic_1164.all;

entity UUT is
    port (
        input_signal1 : in std_logic;
        input_signal2 : in std_logic;
        output_signal1 : out std_logic;
        output_signal2 : out std_logic
    );
end UUT;

architecture rtl of UUT is
begin
    output_signal1 <= input_signal1 and input_signal2;
    output_signal2 <= input_signal1 or input_signal2;
end rtl;
```

## 2. Create a testbench for the UUT.

```
library ieee;
use ieee.std_logic_1164.all;

entity testbench is
```

```
end testbench;
```

architecture tb\_arch of testbench is

```
    signal input_signal1 : std_logic;
```

```
    signal input_signal2 : std_logic;
```

```
    signal output_signal1 : std_logic;
```

```
    signal output_signal2 : std_logic;
```

```
    component UUT
```

```
    port (
```

```
        input_signal1 : in std_logic;
```

```
        input_signal2 : in std_logic;
```

```
        output_signal1 : out std_logic;
```

```
        output_signal2 : out std_logic
```

```
    );
```

```
end component;
```

```
begin
```

```
    UUT_inst : UUT
```

```
    port map (
```

```
        input_signal1 => input_signal1,
```

```
        input_signal2 => input_signal2,
```

```
        output_signal1 => output_signal1,
```

```
        output_signal2 => output_signal2
```

```
    );
```

```
-- Apply stimulus to the UUT
```

```
input_signal1 <= '0';
```

```
input_signal2 <= '1';
```

```
-- Monitor the output signals of the UUT
```

```
process
```

```
begin
```

```
    wait for 10 ns;
```

```
    assert output_signal1 = '0' and output_signal2 = '1'
```

```
        report "Test failed"
```

```
        severity error;
```

```
    wait;
```

```
end process;
```

```
end tb_arch;
```

# Things to note

- The testbench instantiates the UUT and connects the input and output signals.
- Entity block in testbench is empty because we are not using any ports.
- Entity block from UUT re-typed inside architecture block of testbench, entity keyword changed to component keyword.
- Signal input and output signals are declared in the architecture block of the testbench.
- Value changes are applied to the input signals with desired delays.

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