

1. Memory in AVR Architecture

AVR Architecture is an 8 bit single-chip RISC microcontroller with a modified Harvard Architecture that is organized as the following which causes it to behave certain ways when handling memory.

eclipse.umbc.edu - AVR Architecture

“ You don't have to memorize all this don't worry.

There are several memory spaces in this organization, but for now we will look at the two most important ones to know.

Program/Flash Memory

rhjcoding.com - Flash memory When you compile and upload codes (flashing), it's stored in the **Flash Memory** section semi-permanently. During runtime, the control unit fetches instructions from this memory section.

This portion of the memory is non-volatile which means the data stored won't be erased after power loss.

Data Memory - DS (Data Space)

rhjcoding.com - Data Memory The **Data Memory** consists of several memory parts mapped into one contiguous memory addresses.

- **32 General Purpose Registers** (0x0000 - 0x001F)
- **64 I/O Registers** (0x0020 - 0x005F)
- **160 Extended I/O Registers** (0x0060 - 0x00FF)
- **SRAM** (Implementation Specific)

The **Static RAM** (SRAM) is a memory block used to store data used during runtime. One part of this is the stack that may come in handy for temporary data (more on this later).

thecoderscorner.com - SRAM

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