

3. The Status Register

The Status Register (SREG) is a special 8 bit register that saves different operational status flags in each bit. Different operations may affect different flags (bit) of the register which then would be useful to create decisions after.

In AVR architecture, SREG is an I/O register meaning that it can be operated with instructions such as `OUT` and `IN`.



Carry Flag (C) [0]

- Indicates a Carry after addition or a Borrow after subtraction.
- Usually happens when adding up numbers that results in a result greater than 8 bits (255) or when subtracting numbers that results a negative analytically.
- Subtracting a smaller number by a bigger one would result to a negative. This can be used to test whether a number is smaller than the other.

Zero Flag (Z) [1]

- Indicates that the previous operation results a 0.
- Can be set by different arithmetic operations such as `SUB` or `DEC` to logical operations such as `AND`.
- Subtracting two equal values would result in a 0. This property can be used to test if two numbers are equal.

Negative Flag (N) [2]

- Indicates that the previous number results a negative.
- Under the hood works by testing the most significant bit (bit 7, leftmost) which indicates a 2s complement.

Two's Complement Overflow Flag (V) [3]

- Indicates that the previous operation is outside the range of signed values -128 to 127. These two values are the lowest and highest 8 bit signed values.
- Useful for testing overflow during signed 8 bit integer operations.

Sign Flag (S) [4]

- XOR of N and V flag.
- Indicates the sign of the result of the last operation. $S = 1$ means the last operation resulted in a negative signed number.

Half Carry (H) [5]

- Functions like the Carry flag but for only the lower nibbles of the last operation.
- Can come in handy when operating with 4 bit values such as BCD.

Bit Copy Storage (T) [6]

- Unlike the others, can be freely used by the programmer anyway they like.
- Set to 1 with `SET` and 0 with `CLT` instructions.
- Can be used by other registers with `BST Rr, b` and `BLD Rd, b` that moves the 1 bit value of T into or out of bit **b** of register Rr/Rd.
- Technically a free 1 bit storage.

Global Interrupt Enable (I) [7]

- Enables interrupt when set to 1 with `SEI` or disables it when cleared with `CLI`.

Revision #2

Created 2026-02-25 09:06:34 UTC by MF

Updated 2026-02-25 09:07:04 UTC by MF