3. Timer0

3.1. TCNT0 (Timer/Counter 0 Register)

image

The TCNT0 register is the core component of the 8-bit TIMER0 module. It acts as the actual counter that **holds the current timer value**. The value of TCNT0 increments (or decrements in certain PWM modes) based on the **selected clock source** and **prescaler**.

Users can read from or write to this register at any time. Note that manually writing a value to TCNT0 while the timer is running can cause the timer to **"miss" a Compare Match** with the OCR0x registers. This happens because the hardware comparison occurs in the **clock cycle following** a TCNT0 update.

In PWM modes, TCNT0 is **constantly compared** against OCR0A and OCR0B. When the values match, the output pins (OC0A/OC0B) toggle, clear, or set, depending on the configuration.

3.2. TCCR0 (Timer/Counter 0 Control Register)

In the ATmega328P, the control functionality is split into two registers: **TCCR0A and TCCR0B**. Together, they define the timer's behavior, including waveform generation, output modes, and clock scaling.

3.2.1. TCCR0A (Control Register A)

image

- **Bit 7:6** - **COM0A1:0 (Compare Match Output Mode A)**: Controls the behavior of the OC0A pin when TCNT0 matches OCR0A.
- **Bit 5:4** - **COM0B1:0 (Compare Match Output Mode B)**: Controls the behavior of the OC0B pin when TCNT0 matches OCR0B.
- **Bit 1:0** - **WGM01:0 (Wave Generation Mode)**: Combined with WGM02 in TCCR0B to select the timer mode (Normal, CTC, Fast PWM, Phase Correct PWM).

3.2.1.1. COM0x1:0 Description

This table shows the **COM0x1:0 functionality** when the timer is in a **non-PWM mode** (normal or CTC):

COM0x1	COM0x0	Description
0	0	Normal port operation, OC0x disconnected.
0	1	Toggle OC0x on Compare Match.
1	0	Clear OC0x on Compare Match (Set output to low).
1	1	Set OC0x on Compare Match (Set output to high).

3.2.1.2. WGM02:0 Description

This table shows how the **WGM02:0 bits** affect the **counting sequence** of the counter, the source for **maximum (TOP) counter value**, and what **type of waveform generation** to be used:

WGM02	WGM01	WGM00	Timer/Counter Mode of Operation	TOP	Update of OCRx at	TOV Flag Set on
0	0	0	Normal	0xFF	Immediate	MAX
0	0	1	PWM, phase correct	0xFF	TOP	BOTTOM
0	1	0	CTC	OCRA	Immediate	MAX
0	1	1	Fast PWM	0xFF	BOTTOM	MAX
1	0	0	Reserved	—	—	—
1	0	1	PWM, phase correct	OCRA	TOP	BOTTOM
1	1	0	Reserved	—	—	—
1	1	1	Fast PWM	OCRA	BOTTOM	TOP

> **Notes:**
>
> - **MAX**: 0xFF
> - **BOTTOM**: 0x00
> - **Update of OCRx at:** When the hardware actually updates the value of the Compare Register if you change it while the timer is running.

3.2.2. TCCR0B (Control Register B)

image

- **Bit 7** - **FOC0A (Force Output Compare A)**: Only active in non-PWM modes. Writing `1` forces an immediate match on OC0A.
- **Bit 6** - **FOC0B (Force Output Compare B)**: Only active in non-PWM modes. Writing `1` forces an immediate match on OC0B.
- **Bit 3** - **WGM02 (Waveform Generation Mode)**: Works with WGM01:0 to set the mode.
- **Bit 2:0** - **CS02:0 (Clock Select)**: Sets the prescaler or selects an external clock source.

3.2.2.1. CS02:0 Prescaler Settings

CS02	CS01	CS00	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	clk / 1 (No prescaling)
0	1	0	clk / 8 (From prescaler)
0	1	1	clk / 64 (From prescaler)
1	0	0	clk / 256 (From prescaler)
1	0	1	clk / 1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

3.3. TIFR0 (Timer/Counter 0 Interrupt Flag Register)

image

- **Bit 2** - **OCF0B (Output Compare Flag B)**: Set to `1` when TCNT0 matches the value in OCR0B.
- **Bit 1** - **OCF0A (Force Output Compare A)**: Set to `1` when TCNT0 matches the value in OCR0A.
- **Bit 0** - **TOV0 (Timer Overflow Flag)**: Set to `1` when the timer overflows (reaches its MAX value and restarts from 0).

Revision #2
Created 2026-03-03 15:36:43 UTC by RE
Updated 2026-03-03 15:39:12 UTC by RE