

# 4. Timer1

## 4.1. TCNT1 (Timer/Counter Register)

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TCNT1 is **functionally the same as TCNT0**, serving as the core counter for its respective module, with several significant additions and architectural differences. TCNT1 is a **16-bit register** divided into two 8-bit register, **TCNT1H** (high byte) and **TCNT1L** (low byte). This allows it to count from **0 to 65,535**, providing much higher precision and longer timing.

TCNT1 includes a specialized **Input Capture** feature not found in Timer0. When a signal event occurs on the **ICP1 pin**, the current value of TCNT1 is instantly **copied into the ICR1 register**. This is used to measure external pulse widths with high accuracy.

## 4.2. TCCR1 (Timer/Counter 1 Control Register)

### 4.2.1. TCCR1A (Control Register A)

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- **Bit 7:6 - COM1A1:0 (Compare Match Output Mode A)**: Controls the behavior of the OC1A pin when TCNT1 matches OCR1A.
- **Bit 5:4 - COM1B1:0 (Compare Match Output Mode B)**: Controls the behavior of the OC1B pin when TCNT1 matches OCR1B.
- **Bit 1:0 - WGM11:0 (Wave Generation Mode)**: Combined with WGM13:12 in TCCR1B to select one of 16 available modes.

#### 4.2.1.1. COM1x1:0 Description

This table shows the **COM1x1:0 functionality** when the timer is in a **non-PWM mode** (normal or CTC):

COM1x1	COM1x0	Description
0	0	Normal port operation, OC1x disconnected.

COM1x1	COM1x0	Description
0	1	Toggle OC1x on Compare Match.
1	0	Clear OC1x on Compare Match (Set output to low).
1	1	Set OC1x on Compare Match (Set output to high).

#### 4.2.1.2. WGM13:0 Description

This table shows how the **WGM13:0 bits** affect the **counting sequence** of the counter, the source for **maximum (TOP) counter value**, and what **type of waveform generation** to be used:

Mode	WGM13	WGM12	WGM11	WGM10	Timer/Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
0	0	0	0	0	Normal	0xFFFF	Immediate	MAX
1	0	0	0	1	PWM, phase correct, 8-bit	0x00FF	TOP	BOTTOM
2	0	0	1	0	PWM, phase correct, 9-bit	0x01FF	TOP	BOTTOM
3	0	0	1	1	PWM, phase correct, 10-bit	0x03FF	TOP	BOTTOM
4	0	1	0	0	CTC	OCR1A	Immediate	MAX
5	0	1	0	1	Fast PWM, 8-bit	0x00FF	BOTTOM	TOP
6	0	1	1	0	Fast PWM, 9-bit	0x01FF	BOTTOM	TOP
7	0	1	1	1	Fast PWM, 10-bit	0x03FF	BOTTOM	TOP
8	1	0	0	0	PWM, phase and frequency correct	ICR1	BOTTOM	BOTTOM

Mode	WGM13	WGM12	WGM11	WGM10	Timer/Counter Mode of Operation	TOP	Update of OCR1x at	TOV1 Flag Set on
9	1	0	0	1	PWM, phase and frequency correct	OCR1A	BOTTOM	BOTTOM
10	1	0	1	0	PWM, phase correct	ICR1	TOP	BOTTOM
11	1	0	1	1	PWM, phase correct	OCR1A	TOP	BOTTOM
12	1	1	0	0	CTC	ICR1	Immediate	MAX
13	1	1	0	1	(Reserved)	—	—	—
14	1	1	1	0	Fast PWM	ICR1	BOTTOM	TOP
15	1	1	1	1	Fast PWM	OCR1A	BOTTOM	TOP

## 4.2.2. TCCR1B (Control Register B)

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- **Bit 7 - ICNC1 (Input Capture Noise Canceler):** When set to **1**, a digital filter is activated on the ICP1 pin. It requires four matching cycles to trigger, reducing noise spikes.
- **Bit 6 - ICES1 (Input Capture Edge Select):** Selects which edge triggers a capture on the ICP1 pin. **1** = Rising edge; **0** = Falling edge.
- **Bit 3 - WGM13:2 (Waveform Generation Mode):** Works with WGM11:0 to set the mode.
- **Bit 2:0 - CS12:0 (Clock Select):** Sets the prescaler or selects an external clock source.

### 4.2.2.1. CS02:0 Prescaler Settings

CS12	CS11	CS10	Description
0	0	0	No clock source (Timer/Counter stopped)
0	0	1	clk / 1 (No prescaling)
0	1	0	clk / 8 (From prescaler)
0	1	1	clk / 64 (From prescaler)

CS12	CS11	CS10	Description
1	0	0	clk / 256 (From prescaler)
1	0	1	clk / 1024 (From prescaler)
1	1	0	External clock source on T0 pin. Clock on falling edge.
1	1	1	External clock source on T0 pin. Clock on rising edge.

### 4.2.3. TCCR1C (Control Register C)

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- **Bit 7 - FOC1A (Force Output Compare A):** Only active in non-PWM modes. Writing  forces an immediate match on OC1A.
- **Bit 6 - FOC1B (Force Output Compare B):** Only active in non-PWM modes. Writing  forces an immediate match on OC1B.

## 4.3. TIFR1 (Timer/Counter 1 Interrupt Flag Register)

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- **Bit 5 - ICF1 (Input Capture Flag):** Set to  when a capture event occurs on the ICP1 pin.
- **Bit 2 - OCF1B (Output Compare Flag B):** Set to  when TCNT1 matches the value in OCR1B.
- **Bit 1 - OCF1A (Force Output Compare A):** Set to  when TCNT1 matches the value in OCR1A.
- **Bit 0 - TOV1 (Timer Overflow Flag):** Set to  when the timer overflows (reaches its MAX value and restarts from 0).

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