

5. Important ADC Parameters In ATmega328p

5.1 Reference Voltage (Vref)

Reference Voltage (Vref) is the maximum voltage that serves as the full-scale reference in the ADC conversion process. Vref determines the range of input voltage that can be read by the ADC.

On the ATmega328p, there are three options for the reference voltage source:

REFS1	REFS0	Vref Source	Description
0	0	AREF pin	Uses an external voltage connected to the AREF pin
0	1	AVcc	Uses the supply voltage (VCC), typically 5V
1	0	<i>(unused)</i>	—
1	1	Internal 2.56V	Uses a fixed internal 2.56V reference voltage, ignoring VCC

image

Influence of Vref on effective resolution:

Vref	Resolution per step
5V (AVcc)	$5V / 1024 \approx 4.88 \text{ mV}$ per step
2.56V (Internal)	$2.56V / 1024 \approx 2.5 \text{ mV}$ per step

The smaller the Vref, the finer the resolution — but the measurable input range is also smaller.

5.2 Prescaler

The **Prescaler** is a frequency divider that determines the ADC clock speed from the main system clock (F_CPU). The ADC requires a clock within the range of **50 kHz - 200 kHz** for accurate results.

On the ATmega328p (F_CPU = 16 MHz), prescaler options are configured via the **ADPS2:ADPS0** bits in the ADCSRA register:

ADPS2	ADPS1	ADPS0	Divider	ADC Clock (at 16 MHz)
0	0	0	CLK/2	8 MHz
0	0	1	CLK/2	8 MHz
0	1	0	CLK/4	4 MHz
0	1	1	CLK/8	2 MHz
1	0	0	CLK/16	1 MHz
1	0	1	CLK/32	500 kHz
1	1	0	CLK/64	250 kHz
1	1	1	CLK/128	125 kHz □ (most accurate)

“ **Note:** The recommended ADC clock is between 50 kHz–200 kHz. A CLK/128 prescaler at 16 MHz produces 125 kHz — well within the optimal range.

5.3 Conversion Rate

Conversion Rate is the number of ADC conversions that can be performed per second. Its value depends on the ADC clock and the number of clock cycles per conversion.

On the ATmega328p:

- One ADC conversion requires **13 ADC clock cycles** (except for the first conversion after enabling = 25 cycles).
- Conversion Rate = ADC Clock / 13

Prescaler	ADC Clock	Conversion Rate
CLK/64	250 kHz	≈ 19.2 kSPS
CLK/128	125 kHz	≈ 9.6 kSPS

“ **kSPS** = kilo Samples Per Second (thousands of samples per second)

5.4 Influence of Vref, Prescaler, and Conversion Rate on Accuracy

These three parameters are interrelated in determining the quality of ADC conversion results, in terms of resolution, accuracy, and the ability to track signal changes.

Parameter	Smaller Value	Larger Value
Vref	Finer resolution (small LSB), but limited input range	Wider input range, but coarser resolution (large LSB)
Prescaler (divider)	Higher ADC frequency → risk of inaccuracy if exceeding specification limits	Lower ADC frequency → more stable operation if within optimal range (50–200 kHz)
Conversion Rate	Sparse sampling → risk of losing information (aliasing)	More frequent sampling → better ability to track signal changes

Conclusion:

- **Vref** determines the trade-off between resolution and measurement range.
- The **Prescaler** must be chosen so that the ADC frequency stays within the optimal range to maintain accuracy.
- The **Conversion rate** must be high enough ($\geq 2 \times$ signal frequency, according to the Nyquist Theorem which you will learn in the 5th-semester Telecommunications lab) for the signal to be well-represented.

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