

USART Register Architecture of ATmega328p

The ATmega328p microcontroller uses several specific registers to control and monitor USART communication.

1. UBRR (USART Baud Rate Register)

picture 1

A 16-bit register that determines the communication speed. It is divided into two 8-bit registers:

- **UBRR0H:** Stores the 8 most significant bits (MSB).
- **UBRR0L:** Stores the 8 least significant bits (LSB).

The following table provides a reference for **UBRR0** (USART Baud Rate Register) settings corresponding to standard baud rates (bps). It details the required register values for three common oscillator frequencies (**f_{osc}**): 16.0000 MHz, 18.4320 MHz, and 20.0000 MHz. For each frequency, the table accounts for both normal speed (**U2Xn = 0**) and double speed (**U2Xn = 1**) modes, including the resulting percentage error for each configuration.

picture 0

2. UDR (USART Data Register)

picture 2

An 8-bit register that serves a dual purpose:

- **TXB (Transmit Data Buffer):** The location where data to be sent is written.
- **RXB (Receive Data Buffer):** The location where incoming data is read.

3. UCSR0A (USART Control and Status Register A)

picture 3

Used to monitor communication status and configure the speed mode.

| Bit | Name | Description |
|--------------|-------------------|---|
| RXC0 | Receive Complete | Set to 1 if there is new unread data in the UDR. |
| TXC0 | Transmit Complete | Set to 1 if all data has been transmitted. |
| UDRE0 | UDR Empty | Set to 1 if the UDR register is empty and ready for new data. |
| FE0 | Frame Error | Occurs when there is an error in the stop bit. |
| DOR0 | Data Overrun | Occurs when new data arrives before old data is read. |
| UPE0 | Parity Error | Occurs when there is a parity error in the received data. |
| U2X0 | Double Speed | If set to 1, the transmission speed is doubled. |
| MPCM0 | Multi-processor | Enables multi-processor communication mode. |

4. UCSR0B (USART Control and Status Register B)

picture 4

Used to enable the module and interrupts.

- **RXCIE0**: Enables the receive complete interrupt.
- **TXCIE0**: Enables the transmit complete interrupt.
- **UDRIE0**: Enables the data register empty interrupt.
- **RXEN0**: Enables the Receiver.
- **TXEN0**: Enables the Transmitter.
- **UCSZ02**: Additional bit (along with UCSR0C) to determine data size (5-9 bits).
- **RXB80 / TXB80**: Holds the 9th data bit (if using 9-bit format).

5. UCSR0C (USART Control and Status Register C)

picture 5

Used for frame format configuration and operating mode.

- **UMSEL01:0:** Selects the mode (Asynchronous or Synchronous).
- **UPM01:0:** Selects the Parity mode (None, Even, or Odd).
- **USBS0:** Selects the number of Stop Bits (1 or 2).
- **UCSZ01:0:** Determines the data size (paired with UCSZ02 in UCSR0B).
- **UCPOL0:** Clock polarity for synchronous mode.

“ **Note:** When writing to UCSR0C, ensure bit configurations are performed carefully according to the communication protocol requirements of the target device.

Revision #2

Created 2026-02-09 14:21:38 UTC by BH

Updated 2026-02-09 15:06:43 UTC by BH